REMARKS

Claims 1, 3, 7, 8, 14, 18, 22, 24-26, 31, 34, 35, 38, 42, and 43 have been amended, and claims 2, 28-30, and 41 have been cancelled. Accordingly, claims 1, 3-27, 31-40, 42, and 43 are pending in the present application. The claim amendments are supported by the specification, the accompanying figures, and claims as originally filed, with no new matter being added. Accordingly, favorable reconsideration of the pending claims is respectfully requested.

The specification has been amended to add the patent numbers of the issued parent applications.

1. Objections to the Drawings

The drawings have been objected to for failing to show "forming said liner upon said sidewall of said isolation trench comprises deposition of a composition of matter" as recited in claim 4. Applicants respectfully traverse.

This limitation in claim 4 is described at page 12, ll. 14-16 of the specification. "Another method of forming insulation liner 30 is CVD of a dielectric material, or a dielectric material precursor that deposits preferentially upon sidewall 50 of isolation trench 32." Thus, liner 30 in Figures 5A and 5B illustrate the deposition of a composition of matter as recited in claim 4.

Next, "removing said pad oxide" and "forming a gate oxide layer" are shown in Figures 7-8 whereby the pad oxide 14 is removed and the gate oxide layer 44 is added. *See* page 16, ll. 9-14.

Accordingly, Applicants request that the objections to the drawings be withdrawn.

2. Claim Objections

Claims 25 and 34 have been objected to under 37 C.F.R. § 1.75(c) for being of improper dependent form for failing to further limit the subject matter of a previous claim.

The Office Action states that claim 34 recites "a layer composed of polysilicon upon said gate oxide" when it should recite "a layer composed of polysilicon upon said oxide layer."

Regarding claims 25 and 34, however, Applicants respectfully direct the Examiner to Figure 8B, wherein a polysilicon layer 24 is formed over a gate oxide layer 44. The polysilicon layer 24 is formed over the gate oxide layer 44 after the pad oxide layer was removed. *See e.g.* Specification at p. 16, ll. 9-14 and p. 19, ll. 10-16.

Applicants therefore respectfully request the prompt removal of this objection.

3. Objections Under 35 U.S.C. § 132

The amendment filed February 12, 2002 has been objected to under 35 U.S.C. § 132 for allegedly introducing new matter. Applicants respectfully traverse.

Some of the claims have been objected to for including the recitation "said planarizing is performed *in the absence* of masking the conformal layer over each said isolation trench." Operations such as planarizing and selective removing are performed by chemical mechanical planarization or polishing (CMP) in embodiments of this invention that are disclosed in the Application. *See, e.g.*, p. 3, ll. 25-26, p. 6, ll. 1-3, p. 15, l. 4, p. 20, ll. 15-17. The process of CMP does not rely on masking, but rather is used to achieve an overall planar surface, sometimes referred to as global planarity. A rotating table typically holds the wafer in this CMP process and an appropriate slurry is supplied between the wafer and a polishing pad that is applied to the wafer at a specified pressure. Applicants submit that this knowledge of a person of ordinary skill in the art together with the disclosure in the Application of CMP for selective removing and/or

planarizing show possession of the claimed invention.

Accordingly, Applicants respectfully request the prompt removal of the objection under 35 U.S.C. § 132.

4. Rejections Under 35 U.S.C. § 112, First Paragraph

Claims 1, 3-27, 31-40, 42, and 43 have been rejected under 35 U.S.C. § 112, first paragraph, for containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Applicants respectfully traverse.

The Office Action states that there does not appear to be a written description of the claim limitation "planarizing is performed *in the absence* of masking the conformal layer over each said isolation trench." As discussed above, operations such as planarizing and selective removing are performed by CMP in embodiments of the invention that are disclosed in the present application. The process of CMP does not rely on masking, but rather is used to achieve an overall planar surface. Applicants submit that the knowledge of a person of ordinary skill in the art together with the disclosure in the present application of CMP for selective removing and/or planarizing show possession of the claimed invention.

Accordingly, the prompt removal of the foregoing rejection of claims 1, 3-27, 31-40, 42, and 43 under 35 U.S.C. § 112, first paragraph, is respectfully requested.

Claims 4, 16, and 21 have been rejected under 35 U.S.C. § 112, first paragraph, "because the specification . . . does not reasonable provide enablement for *rounding the top edge of trench* by depositing material on the trench surface." Applicants respectfully traverse.

Claims 16 and 23 have been rejected for reciting under 35 U.S.C. § 112, first paragraph, "because the specification . . . does not reasonably provide enablement for the liner 30 being formed by deposit, e.g., CVD, to be confined within each isolation trench." Applicants

respectfully traverse.

Applicants therefore respectfully request the prompt withdrawal of the foregoing rejections of the claims under 35 U.S.C. § 112, first paragraph.

5. Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 1, 3-26 and 31-40 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Claims 14, 18, 24, 35, 26, and 31 have been amended to change the term "material" with "a material" in order to provide sufficient antecedent basis.

Claims 35 and 38 have been amended to replace the terms "electrically insulative material" with "an electrically insulative material" in order to provide sufficient antecedent basis.

Accordingly, Applicants respectfully request that the rejection of claims 1, 3-26 and 31-40 under 35 U.S.C. § 112, second paragraph, be withdrawn.

Claims 9, 10, 12, 13, 26, and 27 have been rejected under 35 U.S.C. § 112, second paragraph, as failing to set forth the subject matter that Applicants regard as their invention

In particular, the office action states that the limitation of claim 9 "wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1," and the like. Applicants respectfully traverse.

Regarding the use of the term "selective to" in the specification, Applicant directs the Examiner to page 15, lines 11-15. That passage states in part, "Reduced island 52 is preferably removed with an etch that is selective to isolation film 36 and spacer 28, leaving an isolation structure 48 that extends into and above isolation trench 32, forming a nail shaped structure

having a head 54 extending above and away from isolation trench 32 upon an oxide layer 44." It is therefore clear that, as used in the specification, the term "selective to" indicates that a material is etched more slowly than other materials. Hence, a correct reading of page 14, lines 14-25 of the specification is consistent with the specification by indicating that "planarization will be selective to isolation film 26." Accordingly, the prompt removal of this rejection is respectfully requested.

Regarding the limitation, "planarizing is performed in the absence of masking the conformal layer over each said isolation trench," Applicants respectfully disagree with the rejection. The section of the MPEP cited by the Examiner states in part:

> The current view of the courts is that there is nothing inherently ambiguous or uncertain about a negative limitation. So long as the boundaries of the patent protection sought are set forth definitely, albeit negatively, the claim complies with the requirements of 35 U.S.C. 112, second paragraph.
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> * * *
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> The mere absence of a positive recitation is not basis for an exclusion.

MPEP 2173.05(i), 8th ed. Rev. 1, (emphasis added). Operations such as planarizing and selective removing are performed by chemical mechanical planarization or polishing (CMP) in embodiments of this invention that are disclosed in the Application. See, e.g., Application, p. 3, ll. 25-26, p. 6, ll. 1-3, p. 15, l. 4, p. 20, ll. 15-17. The practice of CMP does not rely on masking, but it is known in contrast for its use to achieve an overall planar surface, sometimes referred to as global planarity. Applicants submit that this knowledge of a person of ordinary skill in the art together with the disclosure in the Application of CMP for selective removing and/or planarizing clearly delineate the bounds of the claimed invention. Accordingly, the prompt removal of this rejection is respectfully requested.

6. Rejections Under 35 U.S.C. § 103

Claims 1, 3-27, and 31-34 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,097,072 to Omid-Zohoor et al. (hereafter "the '072 patent") in view of U.S. Patent No. 5,387,540 to Poon et al. (hereafter "*Poon*"). Applicants respectfully traverse.

Present claim 1 recites "filling each said isolation trench with a conformal layer . . . so as to define an upper surface contour of the conformal layer" and "planarizing the conformal layer beginning with the upper surface contour of the conformal layer and extending at least to the first dielectric layer and each said spacer." Support for this recitation can be found in the present application in Figures 6A and 6B.

In contrast, the method disclosed in the '072 patent relies on the deposition of a reverse-resist mask 368 over trench regions 356 (*see* the '072 patent, Fig. 3K, col. 4, *ll.* 51-52) to subsequently perform a wet or dry etch to partially remove oxide layer 364 and leave a reduced oxide layer 372 with ridges 373 (*see* the '072 patent, Fig. 3L, col. 4, *ll.* 52-54). It is this reduced oxide layer 372 with oxide ridges 373 that is subsequently treated by chemical-mechanical polishing (planarizing) until silicon nitride layer 344 is exposed (*see* the '072 patent, Fig. 3M, col. 4, *ll.* 54-57, 59-61). Accordingly, the method disclosed in the '072 patent does not teach or suggest planarizing the conformal layer "beginning with the upper surface contour of the conformal layer" as recited in claim 1.

Additionally, present claim 7 recites "filling each said isolation trench with a conformal layer . . . to a first thickness of the conformal layer relative to said spacers and said first dielectric layer" and "planarizing the first thickness of the conformal layer to a second reduced thickness." Support for this recitation can be found in the present application in Figures 6A and 6B.

As discussed above, the method disclosed in the '072 patent relies on the deposition of a reverse-resist mask 368 over trench regions 356 to subsequently perform a wet or dry etch to partially remove oxide layer 364 and leave a reduced thickness oxide layer 372 with ridges 373. It is this reduced thickness oxide layer 372 that is subsequently treated by chemical-mechanical polishing (planarizing) until silicon nitride layer 344 is exposed. Accordingly, the method disclosed in the '072 patent does not teach or suggest "planarizing the first thickness of the conformal layer to a second reduced thickness" as recited in claim 7.

Further, claims 18 and 24-26 recite some form of planarization that is performed in the absence of masking of a conformal layer over at least one isolation trench. In contrast, this feature is clearly not taught or suggested in the '072 patent. Rather, the '072 patent discloses a method that involves masking and etching a conformal layer prior to planarizing the layer.

Poon cannot cure the foregoing deficiencies of the '072 Patent. Thus, claims 1, 7, 18, and 24-26 would not have been obvious over the cited references.

Claims 3-6, 8-17, 19-23, and 27 depend from one of claims 1, 7, 18, and 26, respectively, and include the limitations recited therein. Accordingly, for at least the reasons presented above with respect to claims 1, 7, 18, and 26, claims 3-6, 8-17, 19-23, and 27 are not obviated by the '072 patent in view of *Poon*.

Present independent claim 31 recites "planarizing the *conformal layer* . . . to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces" (emphasis added).

In contrast, the method disclosed in the '072 patent relies then on the deposition of reverse-resist mask 368 over trench regions 356 to subsequently perform a wet or dry etch to partially remove oxide layer 364 and leave a remaining oxide layer 364 with ridges 373. It is this reduced oxide layer 372 with oxide ridges 373 that is subsequently treated by chemical-

mechanical polishing until silicon nitride layer 344 is exposed. Accordingly, the method disclosed in the '072 patent does not *planarize the conformal oxide layer* 364 to produce the structure with an upper surface for each isolation trench shown in Fig. 3M therein. Instead, the '072 patent relies upon a more complicated method with more steps.

Further, claim 31 recites that the planarizing is performed in the absence of masking of a conformal layer over at least one isolation trench. In contrast, this feature is clearly not taught or suggested in the '072 patent. Rather, the '072 patent discloses a more complicated method that involves masking of a conformal layer.

Regarding claim 34, the '072 patent does not teach or suggest forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers, and selectively removing said layer composed of polysilicon to form a portion of at least one of said upper surfaces. Consequently, the '072 patent does not teach or suggest the presently claimed method with the features recited in claim 34.

Poon cannot cure the foregoing deficiencies of the '072 Patent. Claims 32-34 depend from claim 31 and include the limitations recited therein. Accordingly, for at least the reasons presented above with respect to claim 31, claims 32-34 are not obviated by the '072 patent in view of *Poon*.

Applicants therefore respectfully request that the rejection of claims 1, 3-27, and 31-34 under 35 U.S.C. § 103(a) be withdrawn.

Claims 35-40, 42, and 43 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over the '072 patent in view of Wolf, "*Silicon Processing for the VLSI Era*" (hereafter "*Wolf*") for the reasons stated on pages 26-33 of the Office Action. Applicants respectfully traverse.

Claim 35 recites, *inter alia*, "forming a polysilicon layer upon said oxide layer." This polysilicon layer serves as an etch stop in various embodiments of the invention. *See e.g.* page 6, ll. 15-17. The '072 patent has no such teaching or suggestion of this feature of the invention.

Additionally, claims 35, 38, and 42 recite some form of planarization that is performed in the absence of masking of a conformal layer over at least one isolation trench. In contrast, this feature is clearly not taught or suggested in the '072 patent. Rather, as previously described, the '072 patent discloses a more complicated method that involves masking of a conformal layer and other steps.

In addition, present claim 43 recites, *inter alia* and with language variations in each claim, "planarizing the *conformal layer* ... to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces" (emphasis added). In contrast, the method disclosed in the '072 patent relies then on the deposition of reverse-resist mask 368 over trench regions 356 to subsequently perform a wet or dry etch to partially remove oxide layer 364 and leave a remaining oxide layer 364 with ridges 373. It is this reduced oxide layer 372 with oxide ridges 373 that is subsequently treated by chemical-mechanical polishing until silicon nitride layer 344 is exposed. Accordingly, the method disclosed in the '072 patent does not *planarize the conformal oxide layer* 364 to produce the structure with an upper surface for each isolation trench shown in Fig. 3M therein. Instead, the '072 patent relies upon a more complicated method with more steps.

Additionally, present claim 42 recites the use of a single etch recipe to form a planar upper surface from the conformal layer. In contrast, the method disclosed in the '072 patent, as previously noted, uses a multi-step method with different etch recipes to form a planar upper surface.

Wolf cannot cure the foregoing deficiencies of the '072 Patent. Claims 36, 37, 39, and 40 depend from one of independent claims 35 and 38, respectively, and include the limitations recited therein. Accordingly, for at least the reasons presented above with respect to claims 35 and 38, claims 36, 37, 39, and 40 are not obviated by the '072 patent in view of *Wolf*.

Applicants therefore respectfully request that the rejection of claims 35-40, 42, and 43 under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

In view of the foregoing, Applicants respectfully requests favorable reconsideration and allowance of the present claims. In the event there remains any impediment to allowance of the application, which could be clarified in a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney.

Dated this 28th day of May 2004.

Respectfully submitted,

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